

absolute maximum ratings over free-air temperature (unless otherwise noted)

Supply Voltage,  $V_{CC}$  7v

Input Voltage,  $V_{in}$  5.5v

Operating Free-Air Temperature Range 0°C to 70°C

Storage Temperature Range -65°C to 150°C

recommended operating conditions

Supply Voltage,  $V_{CC}$  4.75v to 5.25v

Maximum Fan-Out From Outputs A,B,C, or D (connected in any of the three count modes) 10

electrical characteristics,  $V_{CC} = 4.75v$  to 5.25v,  $T = 0^\circ C$  to 70°C

high speed typical gate propagation delay time,  $t_{pd} = 15$  ns

high-a-c noise margin typically 1v

low power dissipation- 10 mW per gate at 50% duty cycle

low output impedance-less than 100 ohms logical 1 at 100mA

PARAMETER	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage	2			v
$V_{in(0)}$ Logical 0 input voltage		0.8		v
$V_{out(1)}$ Logical 1 output voltage at A,B,C, or D	2.4			v
$V_{out(0)}$ Logical 0 output voltage at A,B,C, or D	0.4			v
$I_{in(0)}$ R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub> , or R <sub>4</sub> logical 0 level input current O(1) O(2) 9(1) 9(2)	1.6			ma
$I_{in(0)}$ Input A logical 0 level input current	3.2			ma
$I_{in(0)}$ Input BD logical 0 level input current	6.4			ma
$I_{in(1)}$ R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub> , or R <sub>4</sub> logical 1 level input current O(1) O(2) 9(1) 9(2)	40			μa
$I_{in(1)}$ Input A logical 1 level input current	80			μa
$I_{in(1)}$ Input BD logical 1 level input current	160			μa
$I_{OS}$ Short circuit current at outputs A,B,C, or D	20	55		ma
$I_{CC(av)}$ Average supply current	32			ma

\* Not more than one output should be shorted to ground at a time

description and typical count configurations

The SN7490P is a high-speed monolithic decade counter consisting of four internally gated and interconnected, dual-rank, master-slave flip-flops. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical zero or to a binary coded decimal (BCD) count of 9. The output from flip-flop A is not internally connected to the succeeding stages permitting operation in three independent count modes.

For use as a binary coded decimal decade counter, the BD input (pin 1) must be externally connected to the A output (pin 12). The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD 9 count for nine's compliment decimal applications.

If a symmetrical + 10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output (pin 11) must be externally connected to the A input (pin 14). The input count is then applied at the BD input (pin 1) and a + 10 square wave is obtained at output A (pin 12).

For operation as a + 2 counter and + 5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the + 2 function. The BD input is used to obtain binary + 5 operation at the B, C, and D outputs. In this mode, the two counters operate independently.

	MMX-1	
	Vox-7	A4475
QTY / UNIT	MODEL USED ON	ASS'Y NO.
APPLICATION		
CODE C	S401-265 (SN7490N)	
NOTICE TO PERSONS RECEIVING THIS DRAWING		
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TRUTH TABLES

BCD COUNT SEQUENCE  
(See Note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET (See Note 2)

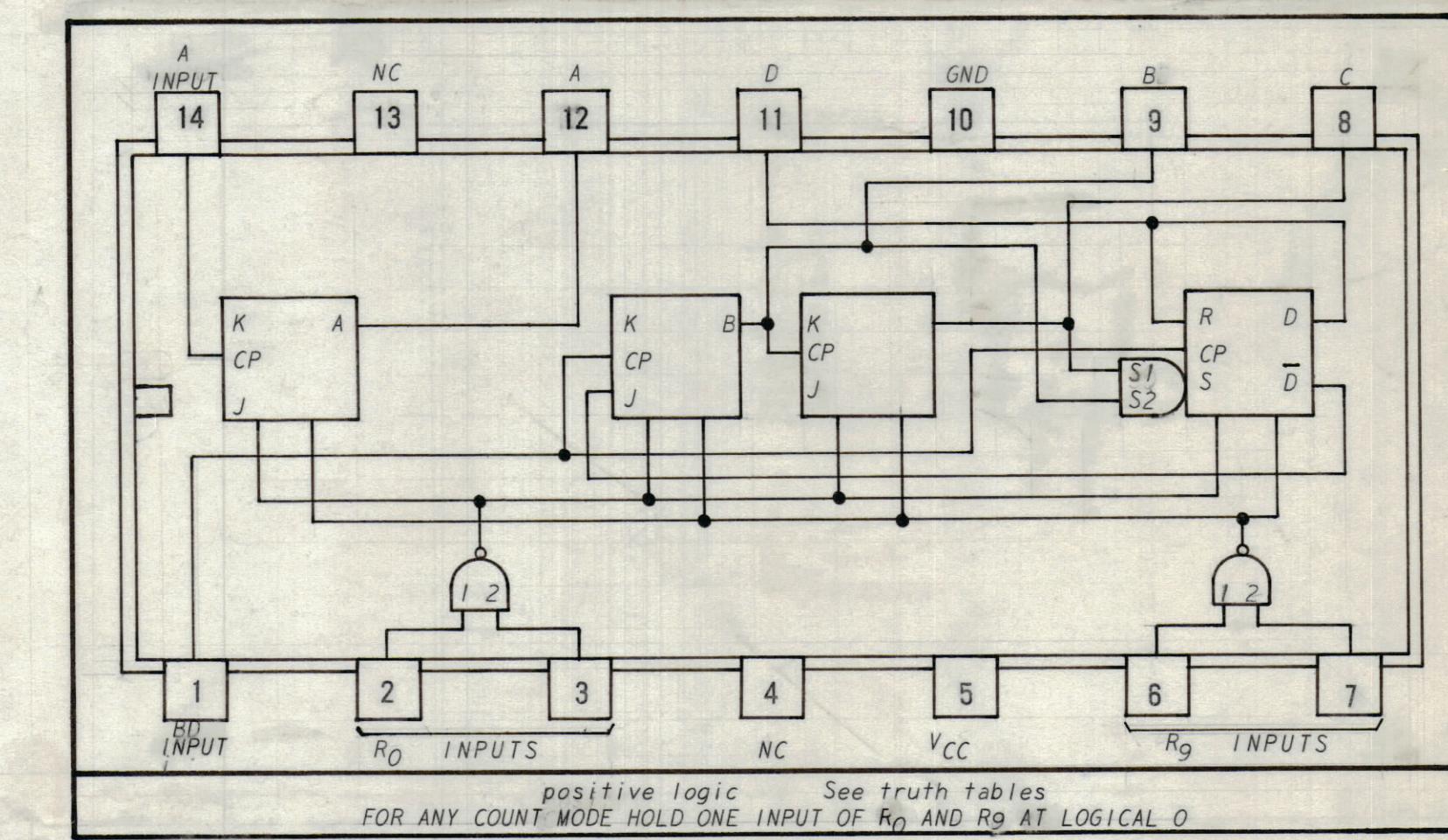
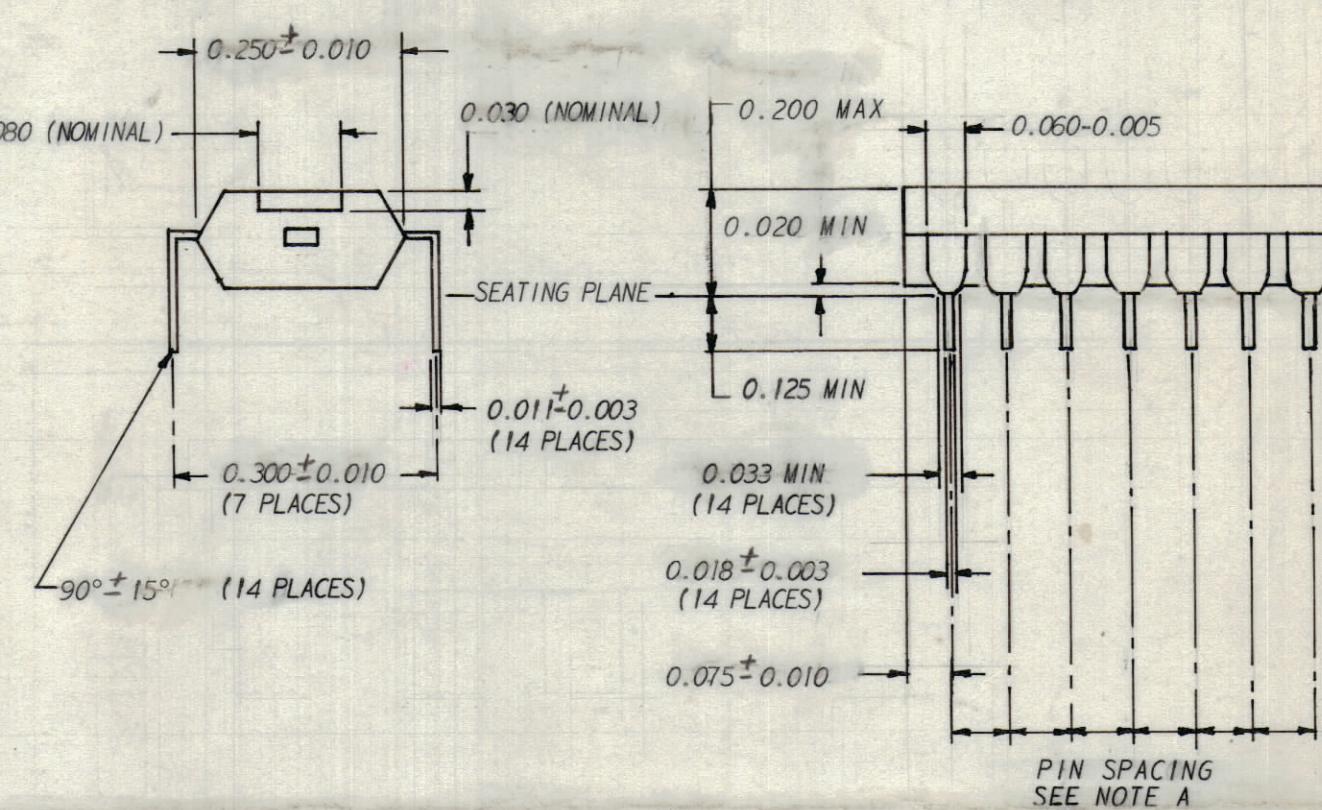
OUTPUT					
R <sub>0</sub>	R <sub>g</sub>	D	C	B	A
0	1	0	0	0	0
1	0	1	0	0	1
2	0	0	1	0	0
3	0	0	1	1	1
4	1	1	COUNT		

NOTES: 1. Pin 1 must be connected to pin 12 for BCD count.

2.  $R_0 = R_g = R$

$O = 0(1) \ 0(2)$  and

$$R = \frac{R}{9(1)} \cdot R_{9(2)}$$



NC- No internal connection

QTY. REQ.	ITEM	PART NO.	DESCRIPTION	SYMBOL
POSE				
LIST OF MATERIAL				
FINAL APPROVAL				
MECH. DES.				
EFFECT. DES.				
CHECKED				
DRAWN				
MATERIAL				
FINISH				
SIZE	CODE IDENT.NO.	DWG. NO.		
C	82679	NW 134		
SCALE	NONE			
SHEET				
OF				

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	E.M.N.NO	DRAFT	CHKD	APPD
X1		MMX-1 ADDED & UPDATED	5-2-67				
8		ORIG RELEASE FOR PRODUCTION	5-25-67	8	RG	Jde	

NOTES: A. The true-position pin spacing is .100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pin 1 and 14.

0.770 MAX

(14) (13) (12) (11) (10) (9) (8)

0.080 R (NOMINAL)  
0.160 (NOMINAL)

(1) (2) (3) (4) (5) (6) (7)

90° ± 15°

PIN SPACING  
SEE NOTE A

positive logic  
See truth tables

FOR ANY COUNT MODE HOLD ONE INPUT OF R<sub>0</sub> AND R<sub>g</sub> AT LOGICAL 0